

WHAT IS CLAIMED IS:

- 1 1. A method of forming a semiconductor device, the method comprising:
2 providing a substrate with one or more shallow trench isolations (STI) formed
3 thereon;
4 forming a protective layer on a first region of the substrate, the first region
5 encompassing a portion of at least one STI;
6 forming one or more semiconductor structures in a second region, the second
7 region not being covered by the protective layer; and
8 removing the protective layer;
9 wherein the portion of the STI located in the second region is partially removed
10 with respect to the STI located in the first region.
- 1 2. The method of claim 1 wherein the semiconductor device is a memory cell.
- 1 3. The method of claim 1 wherein the semiconductor device includes a floating gate
2 transistor.
- 1 4. The method of claim 1 wherein the protective layer is an oxide.

1 5. A method of forming a semiconductor device, the method comprising:
2 providing a substrate with one or more shallow trench isolations (STI) filled with
3 a dielectric material formed therein, the substrate having an oxide layer and a first poly
4 layer formed thereon;
5 forming a protective layer on the first poly layer in a first region of the substrate;
6 fabricating in a second region one or more semiconductor structures, the
7 semiconductor structures utilizing at least one of the first poly layer and the oxide layer in
8 a second region, the second region not being covered by the protective layer;
9 forming on the substrate a second poly layer; and
10 removing the first poly layer, the protective layer, and the second poly layer from
11 the first region.

1 6. The method of claim 5 wherein the dielectric material adjacent to the first region
2 is a different height than the dielectric material adjacent to the second region.

1 7. The method of claim 5 wherein the semiconductor structures include a memory
2 cell.

- 1 8. The method of claim 5 wherein the semiconductor structures include a floating
2 gate transistor.
- 1 9. The method of claim 5 wherein the protective layer is an oxide.
- 1 10. The method of claim 5 further comprising the step of doping the first poly layer in
2 the second region.
- 1 11. The method of claim 5 wherein the step of removing the second poly layer is
2 performed by an anisotropic etching step.
- 1 12. The method of claim 5 wherein the step of removing the oxide layer is performed
2 by an anisotropic etch process.
- 1 13. The method of claim 5 wherein the first region is a periphery region of a memory
2 device and the second region is a cell region of the memory device.

1 14. A method of forming a semiconductor device, the method comprising:
2 providing a substrate with one or more shallow trench isolations (STI) filled with
3 an STI filler formed therein, the substrate having an oxide layer formed on the substrate
4 and a first poly layer formed on the oxide layer;
5 forming a protective layer on the first poly layer and the STI filler in a first region
6 of the substrate;
7 implanting exposed portions of the first poly layer;
8 fabricating in a second region one or more semiconductor structures such that the
9 STI filler located in the second region is partially removed; and
10 removing the protective oxide, and the first poly layer.

1 15. The method of claim 14 wherein the semiconductor device is a memory array.

1 16. The method of claim 14 wherein the semiconductor device includes a floating
2 gate transistor.

1 17. The method of claim 16 wherein the device layers include an inter-poly oxide
2 layer and a gate poly layer.

1 18. The method of claim 14 wherein the protective layer is an oxide.

1 19. The method of claim 14 wherein the first region is a periphery region of a
2 memory device and the second region is a cell region of the memory device.

1 20. The method of claim 14 wherein the step of removing the second poly layer is
2 performed by an anisotropic etching step.

1 21. The method of claim 14 wherein the step of removing the oxide layer is
2 performed by an anisotropic etch process.

1 22. The method of claim 14 wherein the step of removing the protective layer is
2 performed by an anisotropic etch process.

1 23. The method of claim 14 wherein the step of removing first poly layer is
2 performed by an isotropic etch process.